C2S – Circuits & Communication Systems

AxSE Très Grands Réseaux et Systèmes

Smart AMS System for the Data-Driven World & IoE

Coordinator : Patricia Desgreys

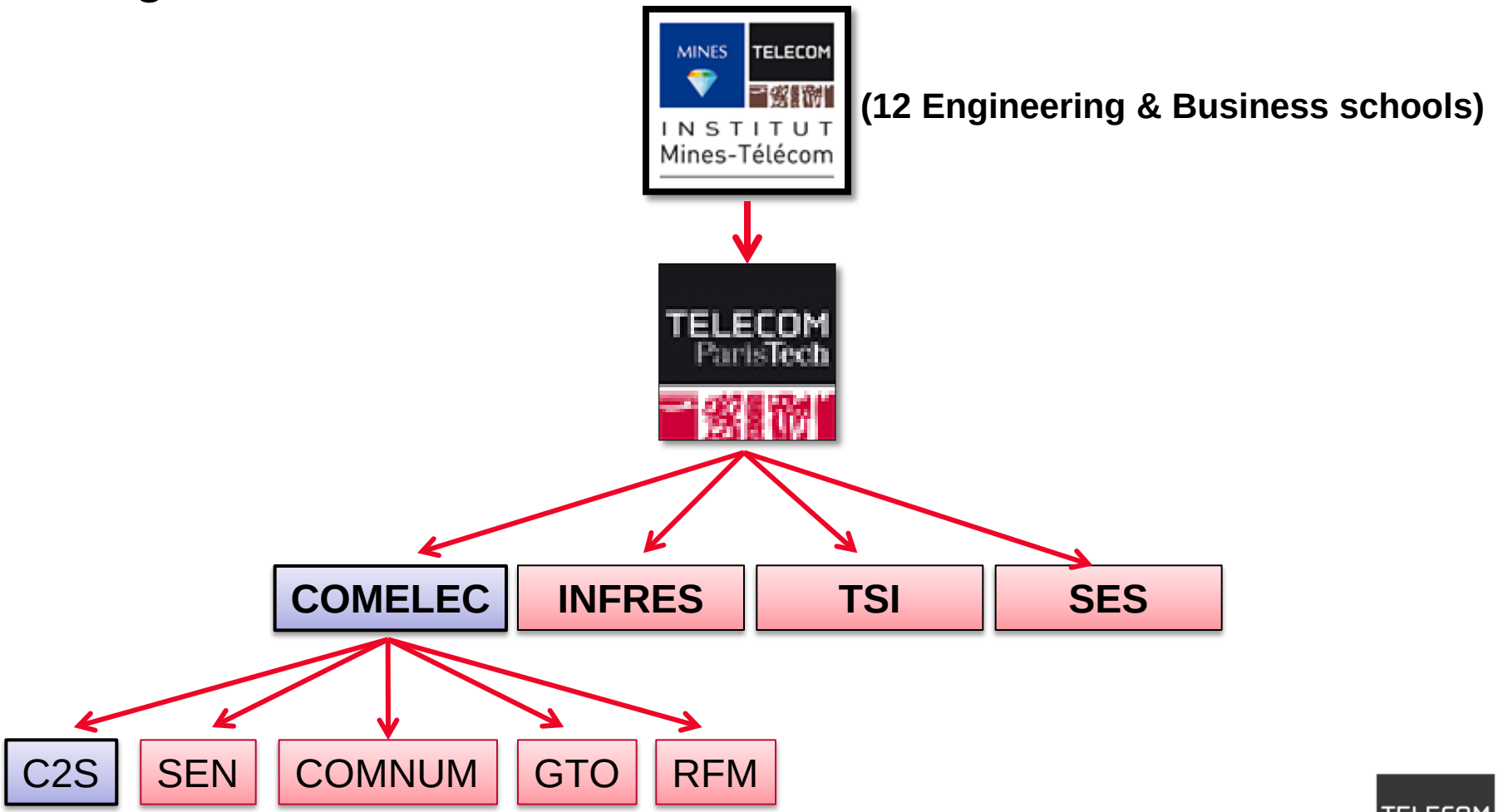
DEPARTMENT COMELEC

CNRS - LTCI

November 2016

Presentation of C2S research group

- **Organization chart**



Presentation of C2S research group

- **C2S team: 5 permanent members, 6 PHD Students, 5 post-doc/CDD**

Pr. Patrick Loumeau
Full professor

Pr. Patricia Desgreys
Full professor

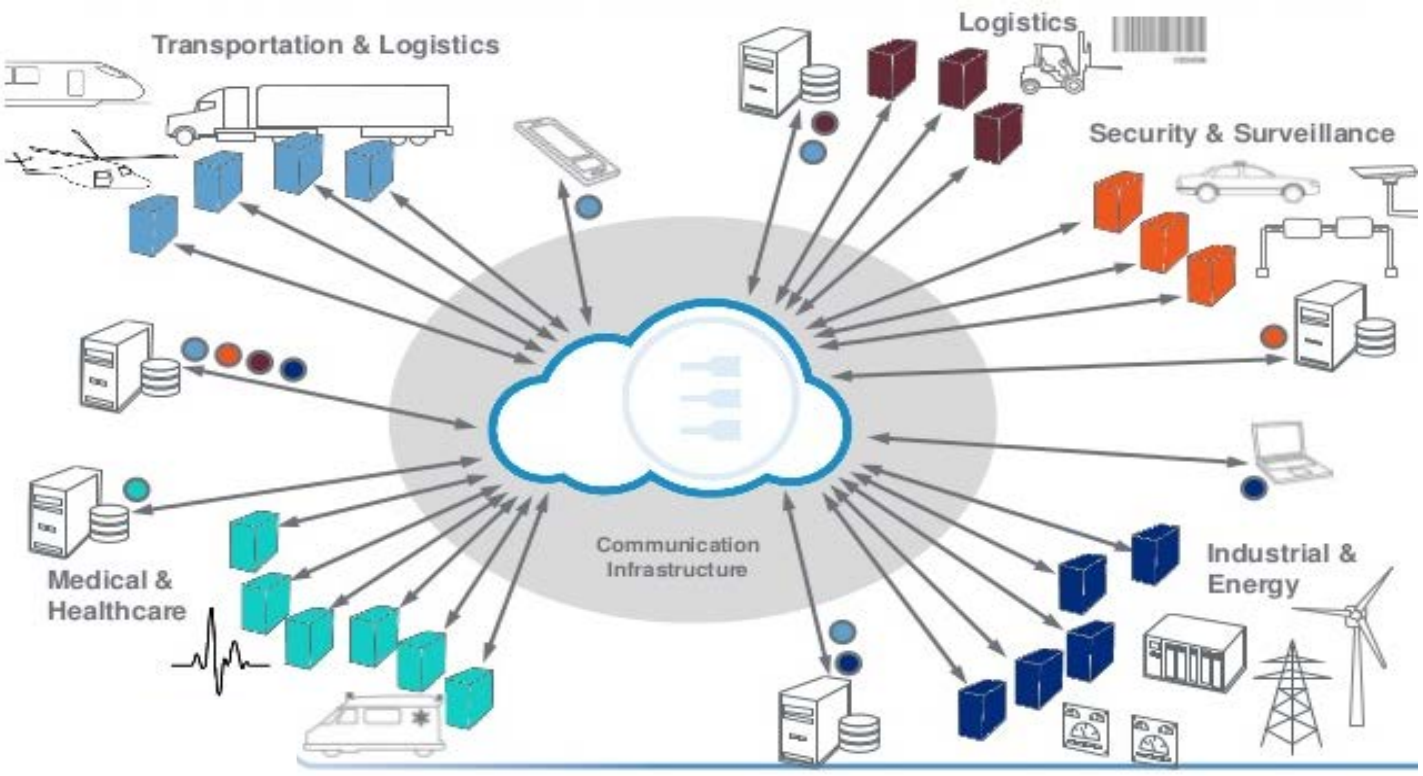
Dr. Hervé Petit
Associate professor

Dr. Van Tam Nguyen
Associate professor

Dr. Chadi Jabbour
Associate professor

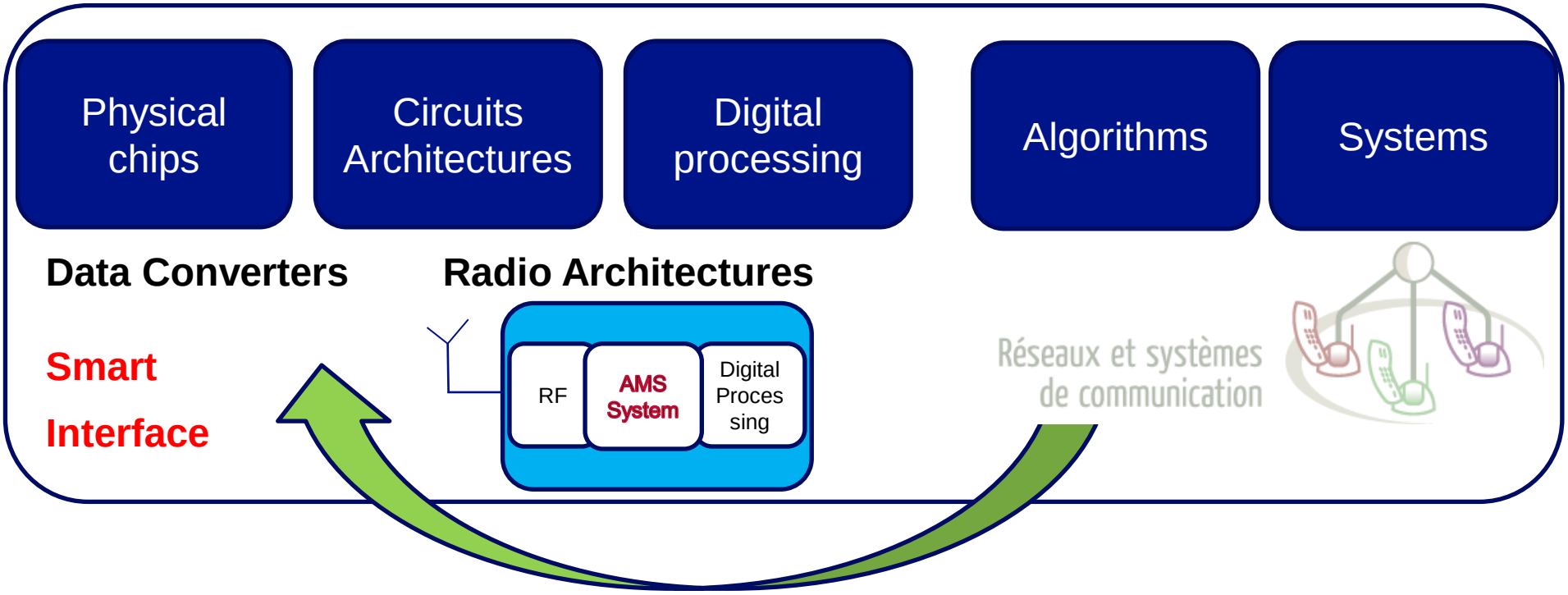
Dr. Germain Pham
research engineer (CDD)

New challenges for the Data-Driven World



Requires smart data & smart and self reconfigurable objects

Smart AMS Systems

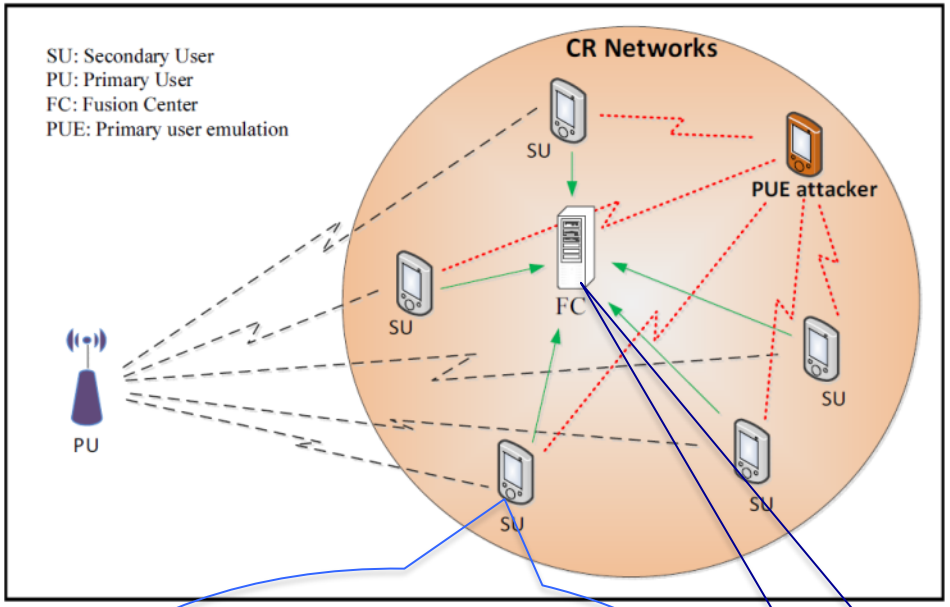


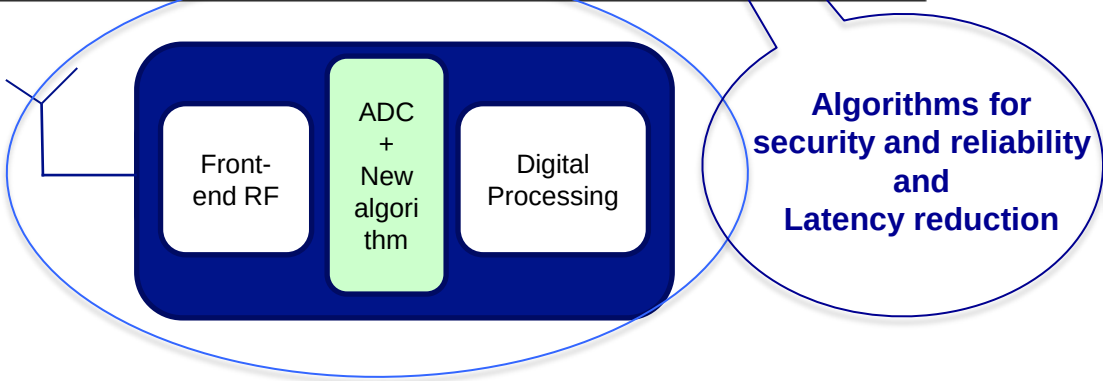
Originality: integrate algorithms in the AMS interface

Cognitive Radio, WSN and IoT

- **Architectural breakthrough**
  - To minimize the power (Joule/information bit)
  - Increase the flexibility (=> digital architecture)

- **Innovative algorithms**
  - Enhance the performance
  - Improve the security and reliability
  - Reduce latency

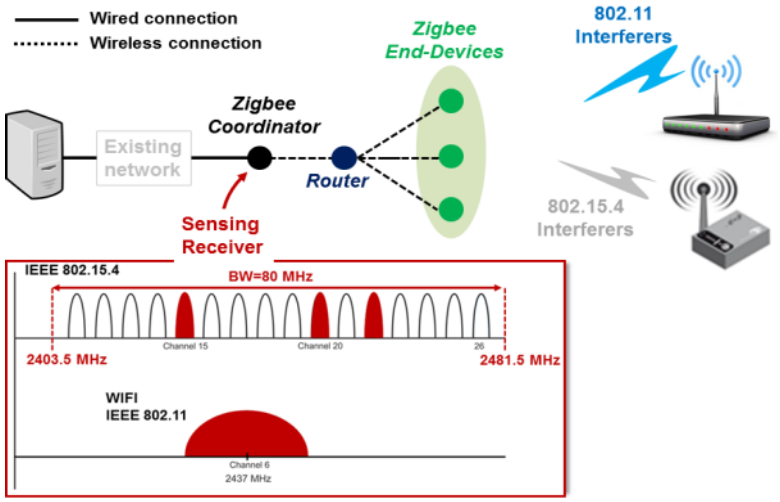


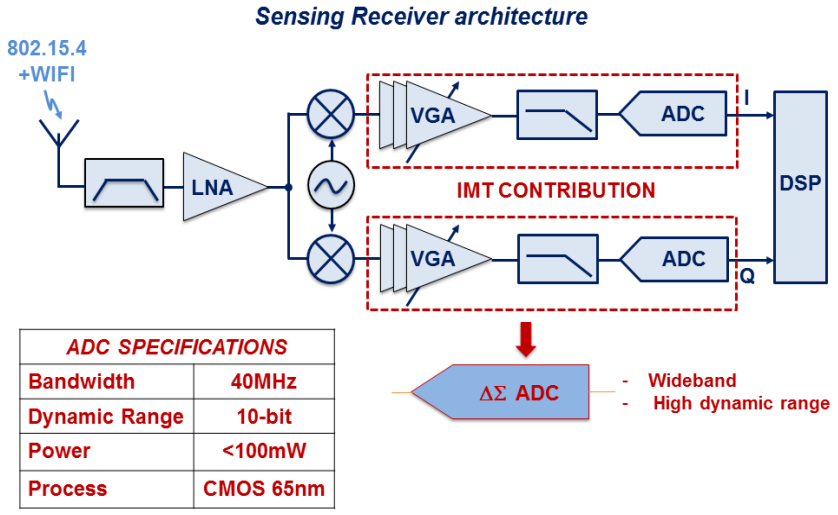


Digital correction algorithms for the non-idealities of the RF front/end

Latest Research Works

P1: Agile Broadband Receivers(CORTIF)

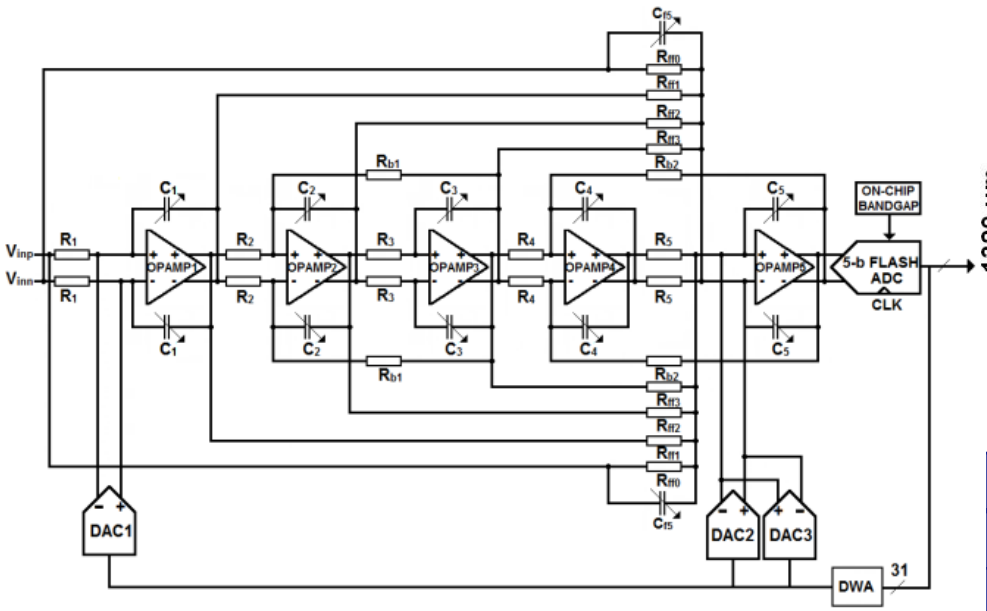


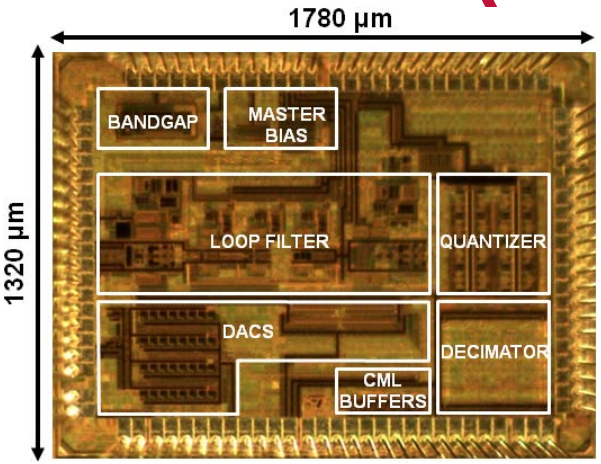


ADC SPECIFICATIONS	
Bandwidth	40MHz
Dynamic Range	10-bit
Power	<100mW
Process	CMOS 65nm

- WSN based on BLE or ZigBee can be impacted by transmissions of other WSN
- The proposed approach consists in using a sensing receiver as a coordinator in order to improve the inter and intra WSN coexistence
- To reduce the receiver cost, analog baseband functions such as VGA and channel filters are replaced by a high dynamic range ΔΣ ADC.

P1:Agile Broadband Receivers(CORTIF)



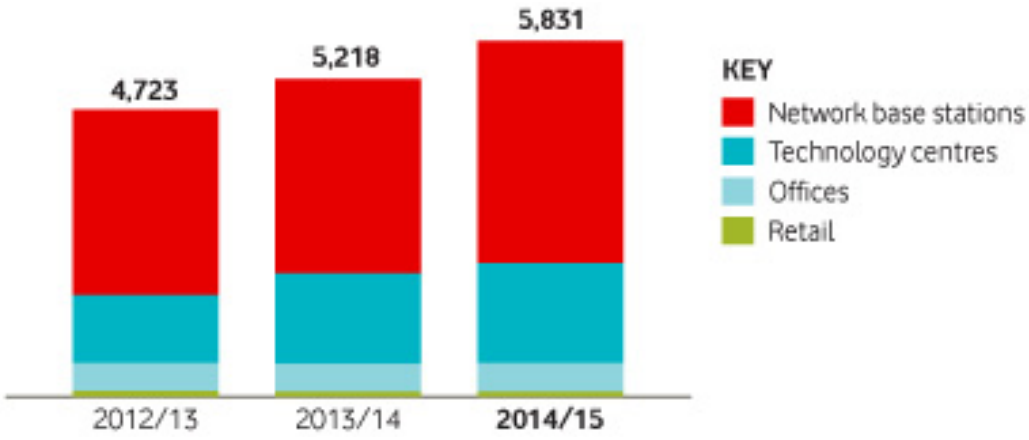


- Single loop CT 5th order modulator
- 5-bit flash with offset calibration
- Time constant calibration for intregrators
- Chip Decimator and Bandgap
- Fabricated in a 1p7M 65 nm CMOS technology from STM

Bandwidth	40 MHz
Fs	640 MHz
Dyn. Range	71.4 dB
Peak SNDR	68,6 dB
Peak SFDR	80 dB
Peak THD	76.5 dB
Power cons. modulator	87.4 mW
Power cons. decimator	12.3 mW
Technology	CMOS 65 nm
Power Supply	1.2V/1V
Core Area	1.7 mm²

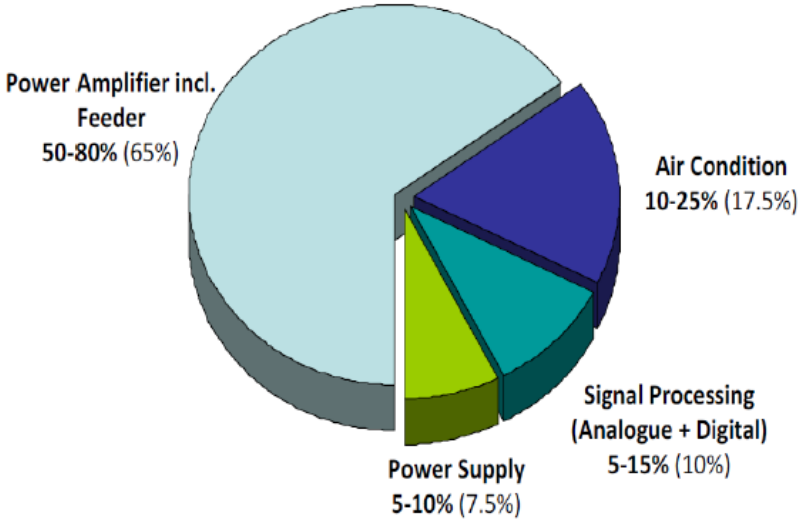
P2: Imp. Power efficiency using pre-distortion

- High energy consumption of current telecom networks



Vodafone energy use (GWh)
Source : Vodafone Sustainability Report 2015

- Energy consumption in base stations



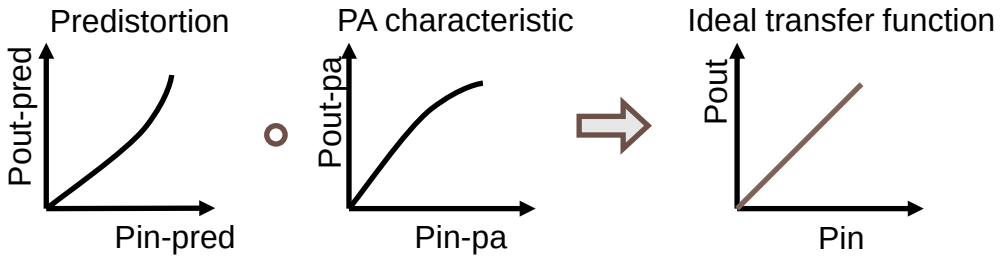
Source : Alberto Conte, Alcatel-Lucent Bell Labs France, “Power Consumption of Base Stations” (Trend Plenary meeting, Ghent, Belgium, February 14-15, 2012)

- Requires greener equipments

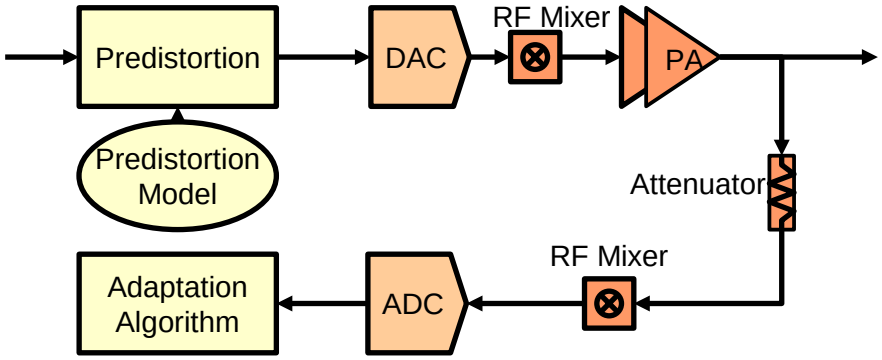
- Requires more efficient PA

P2: Imp. Power efficiency using pre-distortion

- Fundamental idea



- Regular implementation



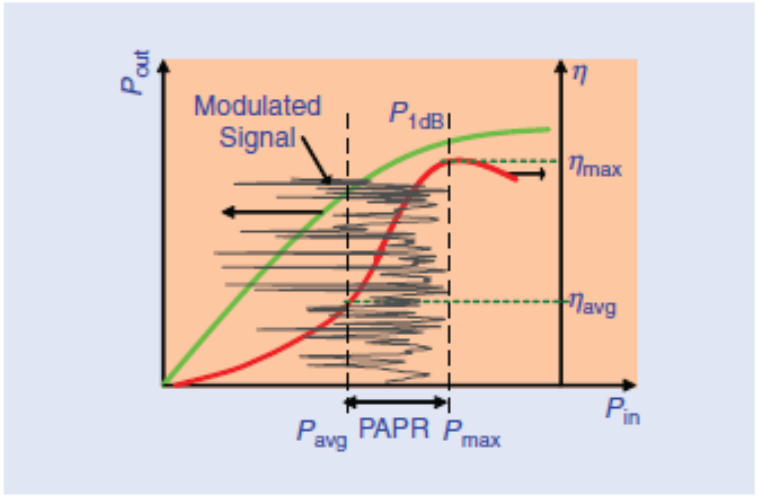


Figure 2. *Output power and efficiency versus input power for one branch amplifier.*

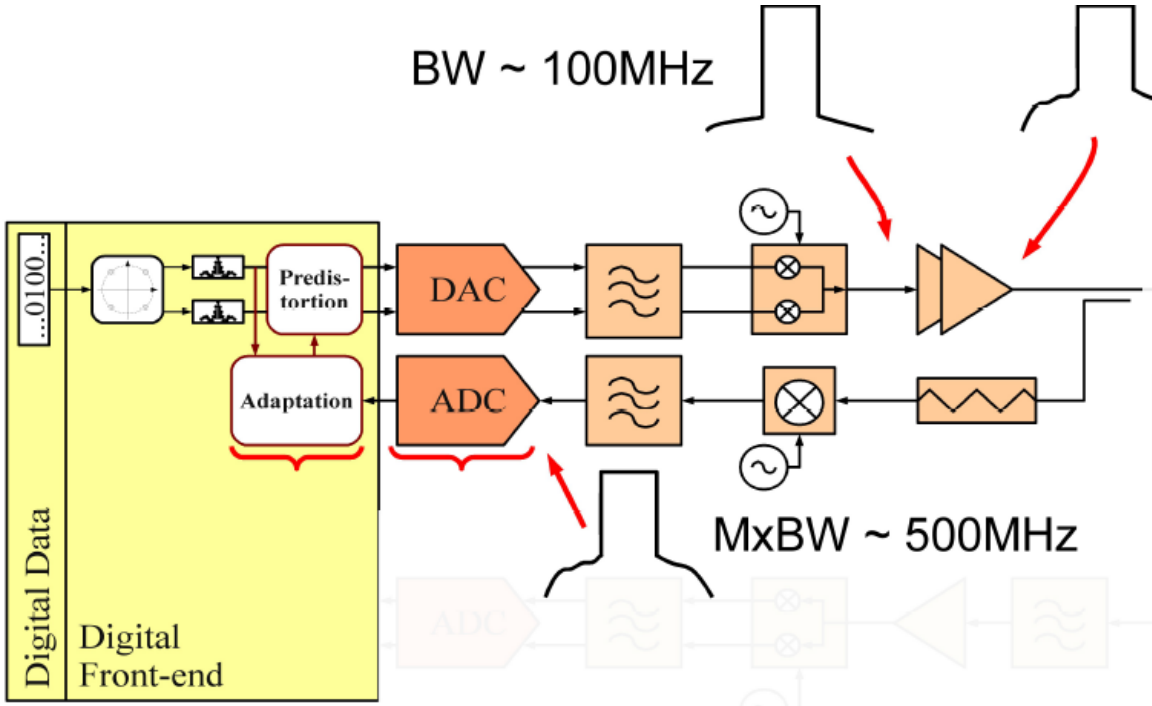
Birafane, A.; El-Asmar, M.; Kouri, A.B.; Helaoui, M.; Ghannouchi, F.M., "Analyzing LINC Systems", 2010.

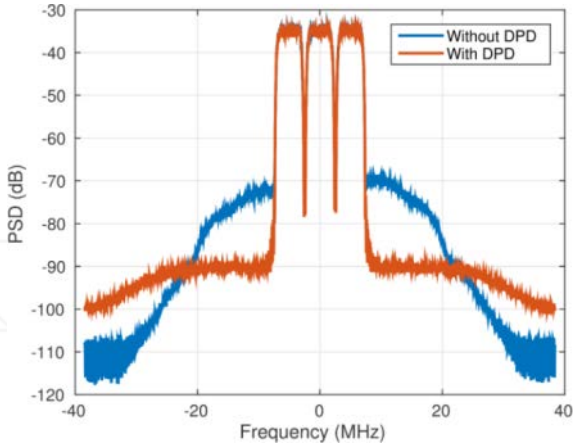
30% increase in power-efficiency of radio transmitters

Digital Predistortion (DPD)

P2: Imp. Power efficiency using pre-distortion

Nanodesign
2014 - 2017



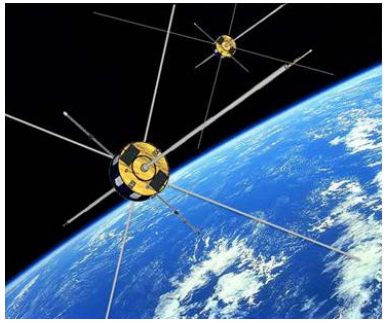


Linearity improvement in term of ACPR

Emerging issues / our proposed solutions :

- **ADC architecture :** Designing new multi-path circuit architecture for ADC
- **Innovate on the DPD algorithm :** Subsampled adaptive algorithm or pruned FFT-based algorithm
- **Trade-off complexity / precision** : Development of a mixed simulation platform

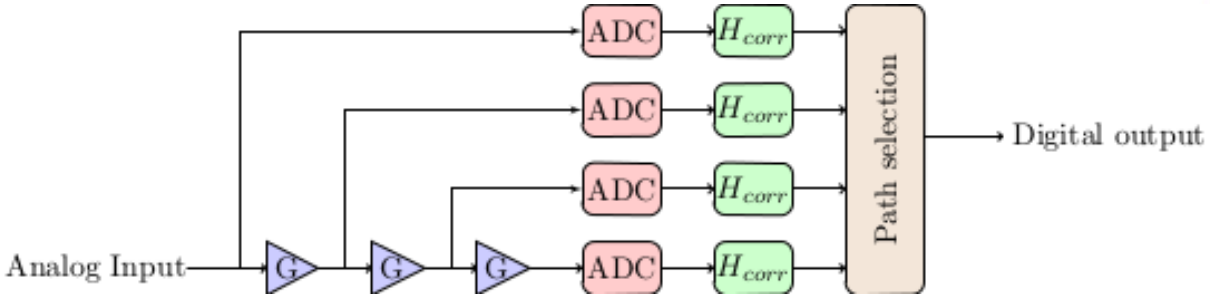
P3-a: Smart data for space astrophysical observations

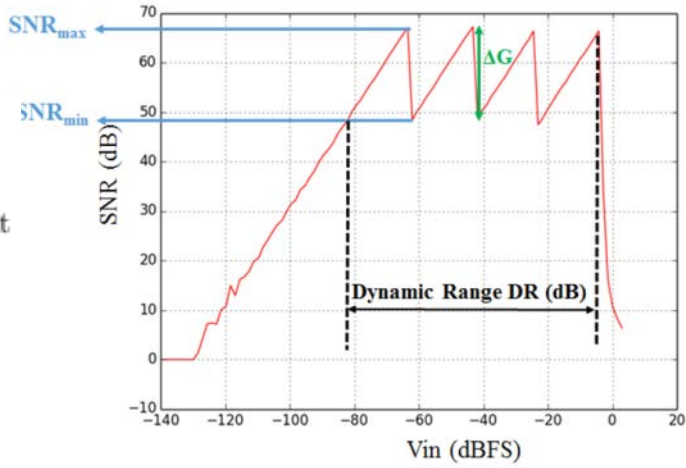


Main objective: Characterize the coupling between the magnetosphere and ionosphere of our planet

Challenges : high DR > 120 dB - BW >50 MHz

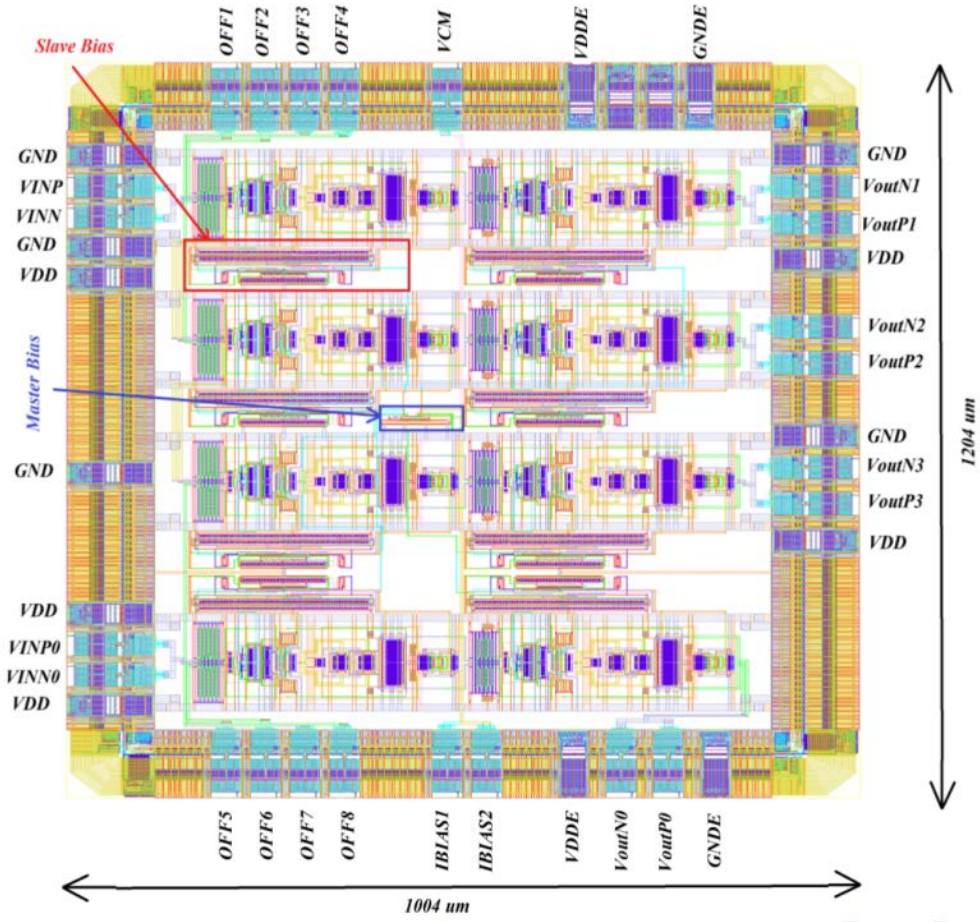
Proposed Solution: Stacked ADC





Overall gain of 90 dB (30 dB/stage) – 10-bit ADC

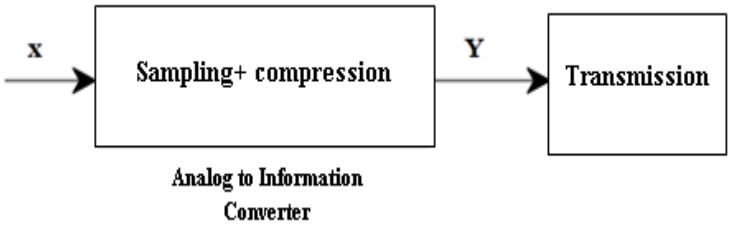
P3-a: Smart data for space astropl observations

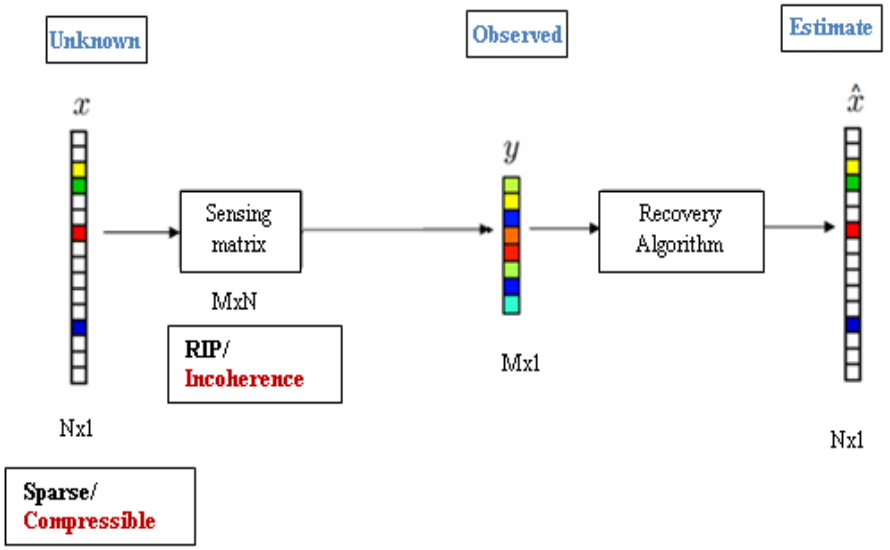


- First Version has implemented just the gain chain, next chip will include the full system
- 3 Channels with 30 dB gain each with a 100 MHz of bandwidth
- A novel calibration algorithm for phase and gain mismatch (off chip)
- Send to fabrication: 1p7M 65 nm CMOS technology from STM

P3-b : Smart data for space astrophysical observations

Emerging sampling paradigm : Compressed Sensing/Compressive Sampling (CS)



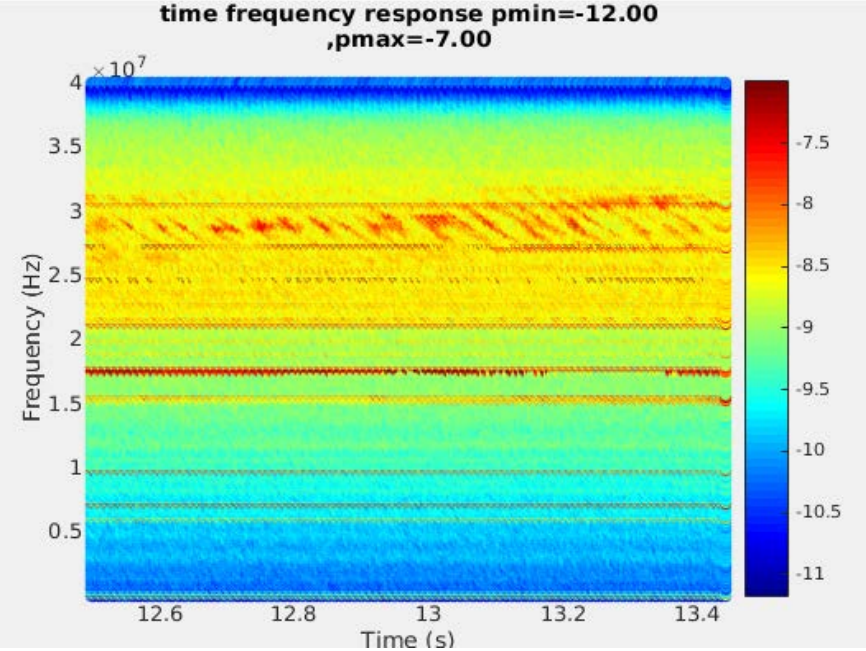


Save resources
- Processing time
- Power consumption
- Storage capacity

Reduce cost

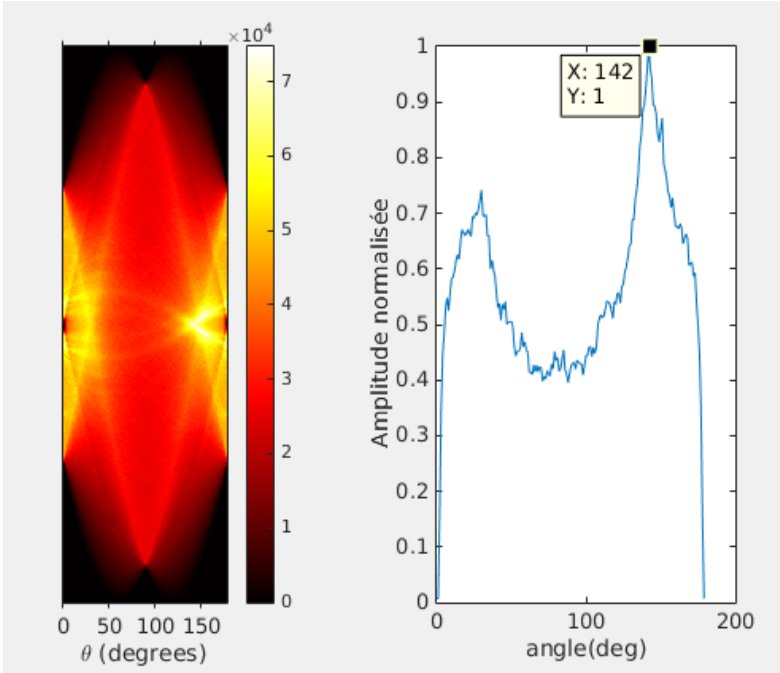
P3-b: Smart data for space astrophysical observations

Signal



Radon Transform

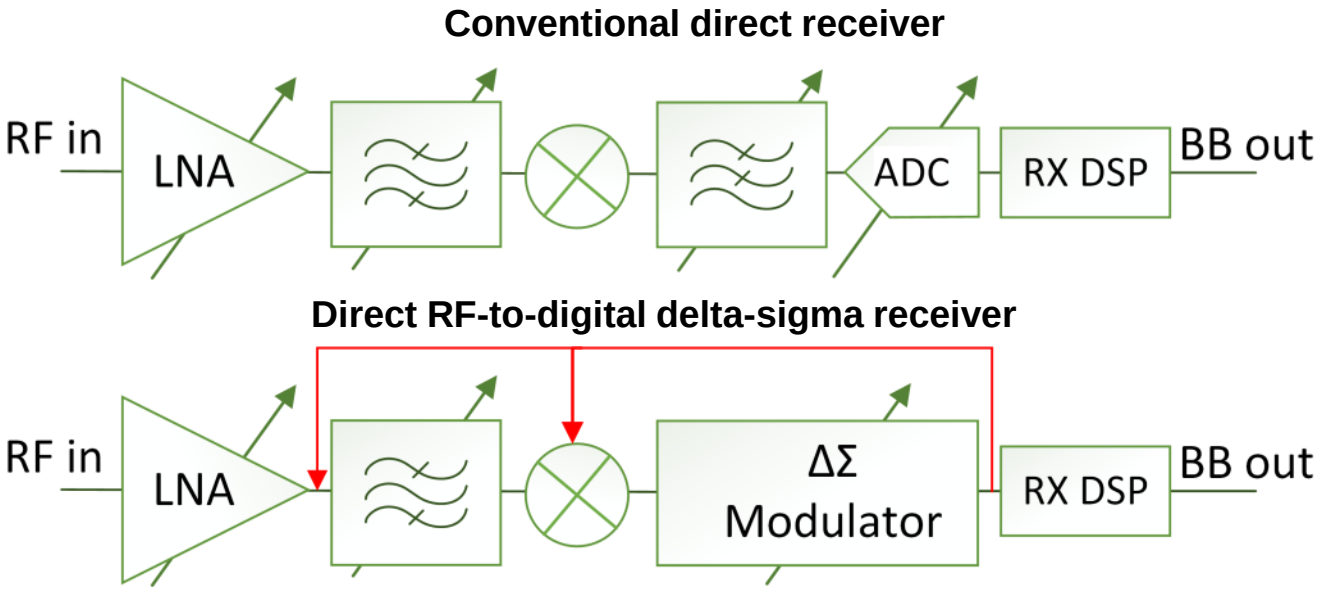
Information



Futur works

- Choice of the sensing matrix
- Proposing an architecture of a radio receiver
- Validation of the proposed structures
- Implementation of the radio receiver demonstrator based on CS

P4: Direct RF-to-digital ΔΣ receiver

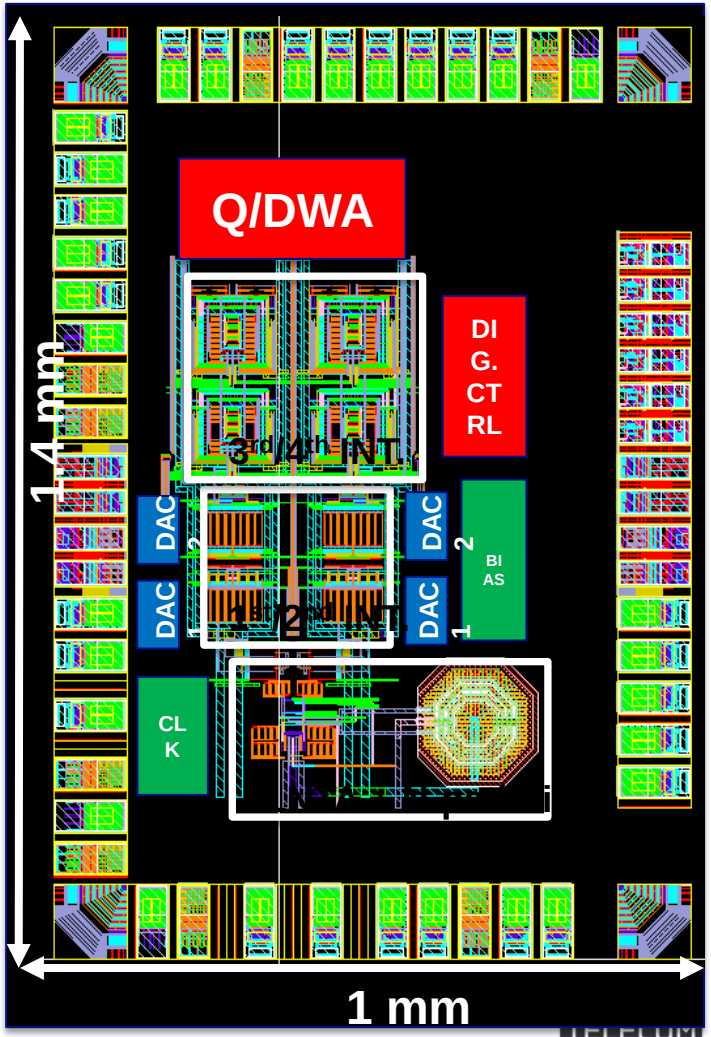


- Direct RF-to-digital delta-sigma receiver (**DDSR**): attractive flexible architecture
- **DDSR promises :**
  - **Compact RF-ADC**
  - **High linearity, high resolution, high flexible**

P4: Direct RF-to-digital ΔΣ receiver

- LO of 0.4 - 6.0 GHz to cover most desirable spectrum [*]
- Discrete-time for high flexible
- Passive front-end for low power consumption
- Fs at LO division for low power consumption
- 4th-order passive/active loop for compromised NF & filtering

'On going' tape-out of the RX



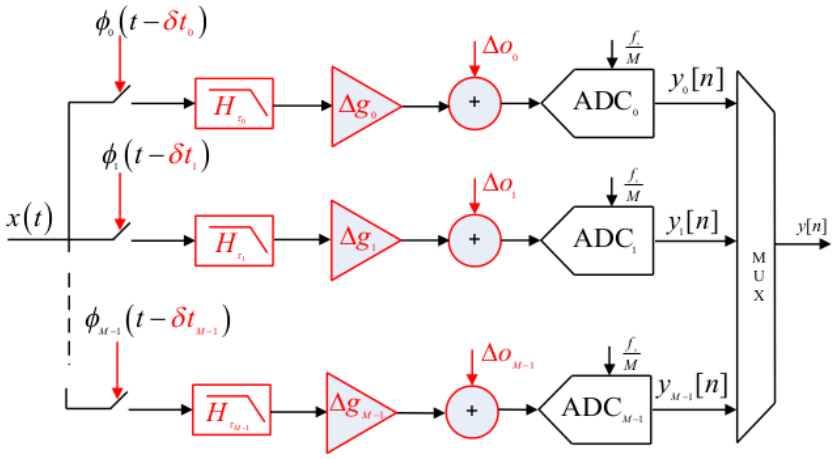
P4: Direct RF-to-digital ΔΣ receiver

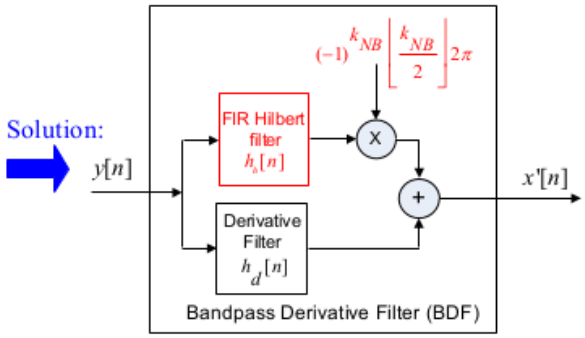
References	[Koli et al. (2010)]	[Englund et al. (2015)]	[Winoto et al. (2009)]	[Wu et al. (2014)]	[Liu et al. (2016)]	This work
System	CT DDSR	CT DDSR	DT DDSR	DT DDSR	CT DDSR	DT DDSR
LO (GHz)	0.9	0.7 – 2.7	0.4-1.7	0.4 - 4.0	0.6 – 3.0	0.4 – 6.0
BW (MHz)	9	15	4	10	10 - 40	10
SNDR (dB)	56	43	55	52 - 64.8	45 – 52	65
RX NF (dB)	6.2	5.9 - 8.8	33	16 - 28.8	2.4 – 3.5	9.0
RX IIP3 (dBm)	4	-2	19	13.5	0	3
Tech. (nm)	65	40	90	65	65	65
Power (mW)	80	90	50.4	17 – 70.5	35.5 – 53.0	48.6 – 78.8 (*) 40.6 – 62.8 (**)

The power consumption: (*) includes/(**) excludes clock input buffers/data output buffers

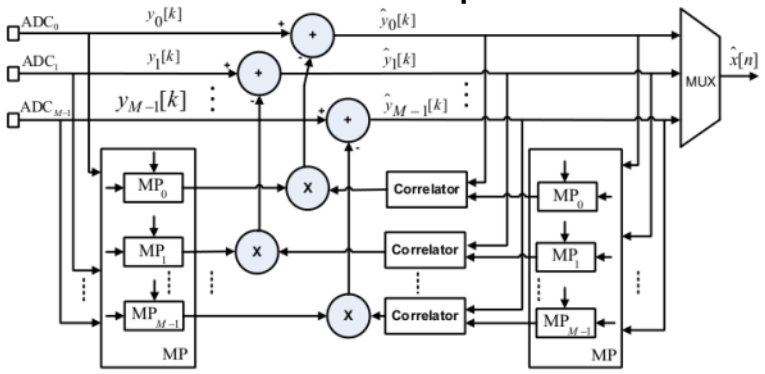
P5: Clock skew Calibration for high speed Time interleaved ADC

Novel approach for undersampling TI ADC





Novel feedforward approach to reduce Power consumption



Static Error:

- Offset.
- Gain.

⇒ Easy to correct.

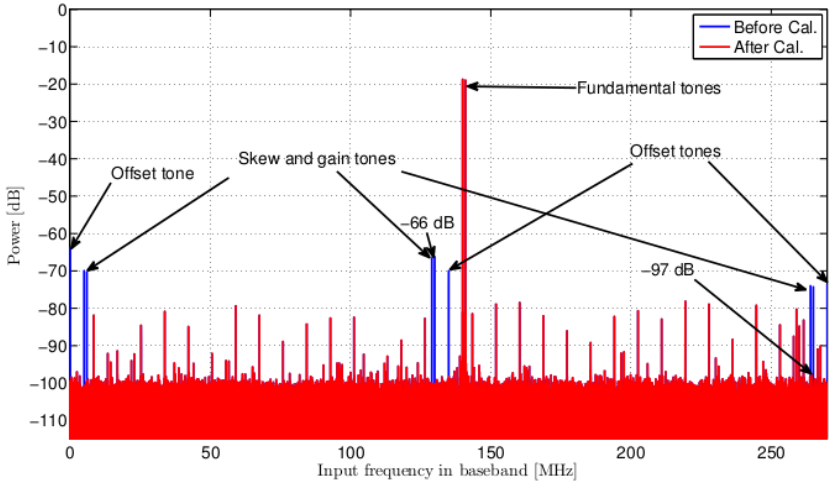
Dynamic Error:

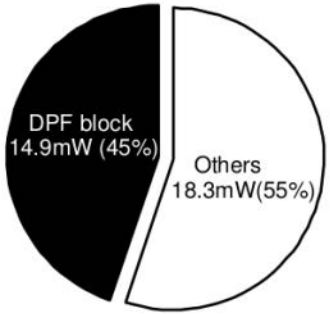
- Clock skews.
- Bandwidth Mismatch.

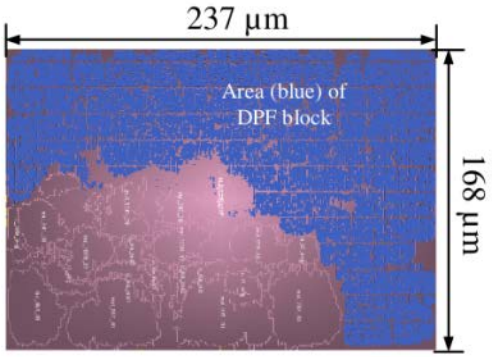
⇒ Focuses on clock skews.

P5: Clock skew Calibration for high speed Time interleaved ADC

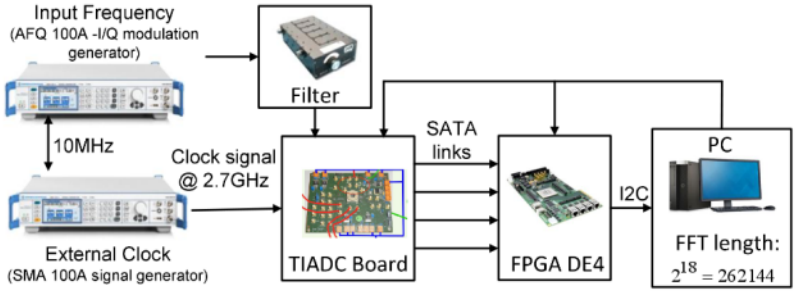
$f_{in} = [2300\text{MHz},\ 2301\text{MHz}]$ with $P_{tone} = -1\text{dBm}$







Meaurement results: skew tones reduced from -46 dBc to -80 dBc (noise floor)



Low power consumption up to the 4th NZ thanks to the feedforward approach

Ref.	This Work	Our previous work [26]	ISSCC 2002 [43]	ISSCC 2014 [10]
Technology	**28nm FD-SOI**	28nm FD-SOI	0.35-μm	40nm
M	**4**	4	2	12
Rate [GS/s]	**2.7**	2.7	0.12	1.6
Resolution	**11 bits**	11 bits	10 bits	12 bits
Input	**Up to NZ4**	Up to NZ4	NZ1	NZ1
Spurs [dBFS]	**97 @ f_{in}[1]**	97 @ f_{in}[1]	90.3 @ 0.99MHz	70 @ 750MHz
Power [mW]	**33.2**	41	171	35.3

[1] $f_{in} = \{2300\text{MHz}, 2301\text{MHz}\}$

Projects

&

Collaborations

Latest Projects

- **PANAMA:** *CATRENE 2009-2012*
- **SACRA:** *FP7 2010-2013*
- **ARTEMOS:** *ENIAC 2011-2014*
- **AppsGate:** *CATRENE 2012-2015*
- **SADIP:** *IDEX-UPSay 2014-2015*
- **CORTIF:** *CATRENE 2014 - 2017*
- **LIFLEX:** *NanoDesign 2014-2017*
- **CORAMED:** *STIC ASIE 2015-2018*
- **CORPA:** *Sen. Marie Curie Fellowship 2015-2018*
- **STAR:** *Col. with LESIA/CNES 2014-2018*

Main Collaborations